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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): BUR920010016US1

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Duane N. Moore

Application Number	Filed
10/060,750	January 30, 2002

First Named Inventor: Robert J. Devins

Art Unit	Examiner
2123	Ayal I. Sharon

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 53-352
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Duane N. Moore
Typed or printed name

(410) 573-6501
Telephone number

May 12, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Ferro et al.

Serial No.: 10/060,750 Group Art Unit: 2123

Filed: January 30, 2002 Examiner: Sharon, Ayal I.

For: SYSTEM FOR CONTROLLING EXTERNAL MODELS USED FOR VERIFICATION OF SYSTEM ON A CHIP (SOC) INTERFACES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTACHMENT TO PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This pre-appeal brief request is being submitted together with a notice of appeal and is in response to the Office Action mailed February 14, 2006, setting a three-month statutory period for response. Therefore, this request is timely filed. Claims 1-34 stand rejected under 35 U.S.C. §102(b) as being anticipated by Blaner, et al., "An Embedded PowerPC SOC for Test and Measurement Applications," 13th Annual IEEE International ASIC/SOC Conference, 2000, September 13-16, 2000, pages 204-208, hereinafter referred to as Blaner. Claims 1-34 stand rejected under 35 U.S.C. §102(e) as being anticipated by Devins, et al. (U.S. Patent No. 6,487,699), hereinafter referred to as Devins. Applicants respectfully traverse these rejections based on the following discussion.

Applicants respectfully traverse these rejections because the rejections contain two clear errors. First, the references miss the claim element of connecting a verification interface model to an (system-on-a-chip) SOC interface. Secondly, the references miss the claim element of a test case in the SOC that can use the same software driver to configure and control both the SOC interface and the verification interface model.

A. Missing Claim Element – connecting a verification interface model to an SOC interface.

Neither of the applied references (Blaner nor Devins) teach connecting a verification interface model to an SOC interface. The Office Action argues that Blaner has the ability to connect a memory-mapped external device, which contains software readable and writable registers that appear as wires in a testbench, to an external bus (Office Action, p. 3, section 10). However, nothing in Blaner mentions connecting the testbench to an external SOC via a verification interface model and a SOC interface. The "memory-mapped external device" of Blaner is not synonymous with the "verification interface model" of Applicants' invention. Specifically, in Blaner, the memory-mapped external device is used to synchronize external activity to internal software. The memory-mapped external device does not connect a testbench to an SOC interface of an external SOC and it does not transfer data to the SOC interface.

To the contrary, as described in paragraph 23 of Applicants' disclosure, the invention transfers data from the verification interface model 210 to the SOC interface 101. The test case calls the software driver (SWD) 135-137 for the interface 101 and instructs the software driver to configure the interface 101 to receive data. Next, the test case calls the same SWD 135-137 and instructs the software driver to configure the verification interface model 210 to send data. The SOC's interface 101 and the verification interface model 210 are implemented to respond to different unique addresses. Thus, when the test case calls the SWD 135-137 to perform some configuration on one of the interfaces, the test case sends the address of that interface along with the operation to be performed. The test case then sends test data to the unique data address of the verification interface model 210. This data is sent from the SOC 100 through the SOC's external bus interface unit (EBIU) 205 to the external EBIU 200 and then along to the verification interface model 210. From there the data is sent through the verification interface model 210 into the SOC's interface 101 which is configured to receive data. Once the data is back in the SOC 100, the test case checks it for correctness and a test status is recorded.

In addition, the Office Action argues that the test operating system (TOS) of Blaner is capable of scheduling test programs for execution and multi-tasking operations, enabling concurrent core execution. This provides the appropriate intercore and bus transactions required for exercising the chip (Office Action, pp. 17-18, section 45(c) (citing Blaner, p. 207, Section IV "Design Verification")). The section of Blaner cited by the Office Action describes the function and performance of the testbench system – it does not disclose the structural elements of an SOC interface and a verification interface model, which connects the testbench to an external SOC.

With respect to Devins, the Office Action proposes that Devins has the ability to couple external bus interface logic of a device to the SOC device via a chip-external bus. However, nothing in Devins mentions connecting the testbench to an external SOC via the verification interface model and the SOC interface. The "external bus interface logic" of Devins is not synonymous with the "verification interface model" of Applicants' invention; rather, as pointed out on pages 12-13, item 28 of the Office Action, "[t]his corresponds to the 'test bench external bus interface unit (EBIU)'".

The Office Action also asserts that Devins expressly teaches an external memory-mapped test device (EMMTD) that is coupled between a SOC design being tested in simulation, and cores external to the SOC design. Further, the Office Action argues that Devins discloses that a test case being executed for SOC verification by a simulated embedded processor in the SOC can communicate with and control elements external to the SOC, by using the EMMTD to perform such functions as initiating external core logic which drives test signals to an internal core, directly controlling an internal core via its external interface, or determining the status of an external core. Although Devins broadly discusses an SOC coupled to external components, Devins does not teach connecting the testbench to an external SOC via the SOC interface and the model interface.

More specifically, as illustrated in FIG. 1 of Applicants' disclosure, the SOC 100 is connected to the verification test bench 300. This connection is made by connecting the SOC interface 101 (of the SOC 100) and the verification interface model 210 (of the

verification test bench 300). Moreover, as described in paragraph 25 of Applicants' disclosure, "[i]n FIG. 1, the invention transfers data from the external interface model 210 to the SOC interface 101 ... the data is sent through the interface model 210 into the SOC's interface 101 which is configured to receive data. Once the data is back in the SOC 100, the test case checks it for correctness and a test status is recorded." Thus, Applicants respectfully submit that, unlike the claimed invention, neither Blaner nor Devins teaches connecting the verification interface model to the SOC interface.

B. Missing Claim Element – a test case in the SOC that can use the same software driver to configure and control both the SOC interface and the verification interface model.

Neither of the applied references (Blaner nor Devins) teach a test case in the SOC that can use the same software driver to configure and control both the SOC interface and the verification interface model. The Office Action argues that Blaner has the ability to use an EBIU to control up to eight banks of mixed types of memories and to operate at one-half the PLB clock frequency (Office Action, pp. 3-4, section 10). Further, the Office Action asserts that Blaner explains that the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories. However, nothing in Blaner mentions a test case in the SOC that can use the same software driver to configure and control both the SOC interface and the verification interface model.

To the contrary, as described in paragraph 24 of Applicants' disclosure, the invention allows the test case executing in the SOC 100 to use the same software driver, if appropriate, to program both interfaces 101, 210. This is an improvement over the conventional situation where the test case running within the SOC 100 controls the SOC interface 101, and another software program (written in a bus functional language) controls the verification interface model 210. The claimed invention provides increased reusability and decreased development time because the system and method uses the same or similar software written in the same language to program both interfaces.

Furthermore, as described in paragraph 26 of Applicants' disclosure, the claimed

invention represents a clean way of controlling external interfaces without the need for a complex control mechanism such as the conventional semaphore derived scheme used to enable communication between the SOC being tested and the external interface. The external bus mastering of the test bench EBIU 200 allows external model programming from the SOC test case. Thus, the same test case directly controls operations of the SOC interface 101 and the verification interface model 210.

Nothing in Blaner teaches the foregoing features of Applicants' invention, namely a test case in the SOC that can use the same software driver to configure and control both the SOC interface and the model interface. The fact that Blaner discloses, on page 205, column 2, paragraph 3, an external bus master for taking ownership of the external bus and accessing attached memories has nothing to do with configuring and controlling both the SOC interface and the verification interface model with the same software driver.

The Office Action also highlights Devins' external bus interface logic 202, which is designed to direct signals received via connection 107 to the appropriate logical address, and to convert the particular bus protocol received into an internally-used format applicable to the command decode logic 203 (column 4, lines 15-20 and 38-40; column 5, lines 5-8). Once more, the features cited in the prior art reference have nothing to do with utilizing the same software driver to configure and control the SOC interface and the verification interface model.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 5/12/06

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